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Analysis of Variable Frequency Drive for Electric Vehicles

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Abstract— Efficient power electronics are critical in electric vehicle powertrains to optimize motor controls. Traditional traction topologies suffer from high switching losses and design complexities due to intermediate DC-DC boost stages. This paper evaluates the operational boundaries of a three-phase Variable Frequency Drive. Developed within the PSpice, the simulation maps the structural trade-offs between 180° and 120° conduction topologies under variable resistance-inductance load lines. Results show that while the 180° mode maintains line voltage stability across all loads, it poses a severe risk of phase-leg shoot-through short circuits during switching intervals. Conversely, the 120° mode prevents shoot-through by providing an inherent 60° non-conducting safety window. The parametric sweeps show that under a heavy inductive load line, the 120° voltage waveform collapses into an asymmetric triangular profile. Furthermore, transient testing indicates that open-loop Piecewise Linear modulations result in severe gate pulse overlap. These findings establish critical boundary constraints vital for deploying secure vehicle inverter drive control loops.

Keywords: *Conduction topologies, electric vehicle, variable frequency drive*

1. INTRODUCTION

The global transition toward electric vehicles (EVs) requires high-efficiency power electronic traction drives to maximize vehicle range and system efficiency [1], [2]. Conventional architectures employ a dual-stage layout, using a standalone intermediate DC-DC boost converter to step up the battery terminal voltage before feeding a three-phase Variable Frequency Drive (VFD). While effective for voltage scaling, this separate boost stage increases design complexities and high-frequency switching losses. To mitigate these hardware integration constraints, single-stage three-phase VFDs are a reliable alternative for directly interfacing the DC source to AC traction motors [3] [4]. In these single-stage configurations, the choice of semiconductor gating topology dictates the hardware's structural reliability and the quality of the output power [5]. The two foundational control sequences used to trigger the bridge semiconductor switches are the 180° and 120° conduction modes [7]. Both configurations exhibit distinct operational characteristics: the 180° mode maximizes DC rail utilization, whereas the 120° mode introduces a non-conducting interval to prevent simultaneous phase-leg conduction [7].

A critical gap in existing power electronics literature is the lack of detailed comparative mapping regarding how these fundamental conduction modes behave under varied load impedances under open-loop conditions. Most contemporary research focuses immediately on complex closed-loop algorithms such as Field-Oriented Control (FOC) or Space Vector Pulse Width Modulation (SVPWM), bypassing the baseline hardware constraints and transient behaviors. This paper addresses the identified research gap by establishing an operational boundary framework for both the 180° and 120° conduction topologies. Using PSpice simulations, this study evaluates the structural behavior of a three-phase inverter bridge subjected to multi-tiered resistance-inductance (R-L) load lines, variable operating-frequency channels, and altered gating pulse widths.

2. BACKGROUND OF THE STUDY

To evaluate the structural trade-offs of a single-stage three-phase VSI, the underlying physics of the semiconductor triggering sequences must be established. The inverter bridge utilizes six voltage-controlled

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switches operating in a complementary sequence across three-phase legs (A, B, C) as shown in Fig. 1 . The output line-to-line voltage equations and current pathways are directly dictated by the conduction interval allocated to each active switch [6].

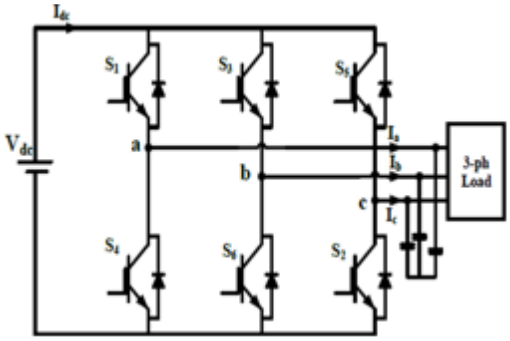

Fig. 1. Circuit diagram of 3-phase VFD

2.1 180° Conduction Mode

In the 180° conduction configuration, each semiconductor switch conducts for a full half-cycle duration. At any given instance, exactly three switches across the bridge remain active simultaneously. The switching sequence changes at 60° intervals, generating a balanced three-step quasi-square line-voltage waveform. The primary mathematical advantage of this mode is its high efficiency in utilizing the DC rail Vdc input. However, when upper and lower switches are on the same phase leg transition instantaneously, the topology introduces a critical vulnerability to phase-leg shoot-through short circuits if gating pulse timings overlap during dead-time failures [6]. The timing diagram is shown in Fig. 2.

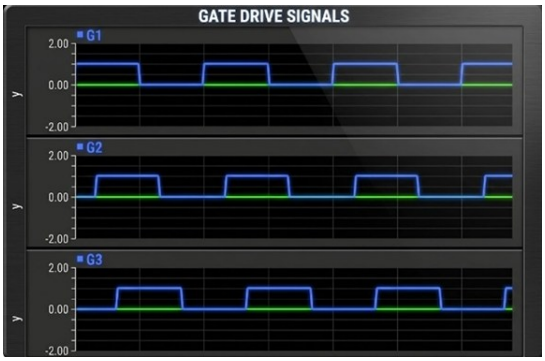

Fig. 2. 180° mode pulse

2.2 120° Conduction Mode

In the 120° conduction configuration, each active switch is gated to conduct for exactly one-third of the total cycle period, as shown in Fig. 3. Therefore, only two switches conduct simultaneously at any single operating window [8]. This mode enforces an inherent 60° non-conducting window per cycle, providing a structural 30° safety dead-time margin. While this safety dead time inherently eliminates the risk of phase-leg shoot-through, the output line voltage assumes a six-step stepped waveform that is highly dependent on the connected load line [3].

2.3 Inductive Load Interactions and Wave Deformation

When feeding a balanced delta-connected resistance-inductance (R-L) load, the current waveform does not instantly follow the voltage steps due to inductive reactance. The stored magnetic energy must be discharged through the anti-parallel freewheeling diodes during unexcited intervals [8]. Under extreme inductive conditions, this continuous freewheeling current discharge forces a geometric collapse of the active voltage steps, shifting the envelope from a staircase profile to an asymmetric triangular wave, thereby inducing high-order harmonic distortions in traction systems [4].

Fig. 3. 120° mode pulse

3. METHODOLOGY

The paper identifies variable-frequency drive (VFD) requirements and then develops the three-phase inverter bridge circuit layout using Capture software. This schematic configuration is subsequently imported into PSpice to execute time-domain transient simulations. Within the simulation environment, multi-variable parametric sweeps are systematically conducted to evaluate different gating conduction modes and alternative modulation coordination methods across variable resistance-inductance (R-L) load-line configurations. Finally, the simulated line-to-line output voltage waveforms are extracted and evaluated to assess signal integrity, underdamped switching transients, and geometric variations before considering the overall operational boundaries and hardware constraints.

The simulation framework was designed in the PSpice environment to analyze the transient and steady-state performance of a three-phase voltage-source inverter (VSI) bridge driving a balanced R-L load, as shown in Fig. 4. The schematic architecture consists of six voltage-controlled semiconductor switches modeled with low on-state resistance parameters to simulate a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [6]. Each active switch is paired with an antiparallel freewheeling diode to permit inductive current to circulate and ensure safe energy dissipation during transition intervals. The DC input rail (Vdc) is maintained at a constant 250V baseline to energize the load network.

3.1 Gate Pulse Sequences

Independent pulse generators control the MOSFET triggering profiles, synchronized to a precise 120° phase shift across the three-phase output legs (A, B, C). Both modes are tested with a variation of loads.

- *180° Conduction Mode:* Controlled via pulse widths set to exactly 10 ms at a 50 Hz frequency, ensuring continuous gating over half the operational period.
- *120° Conduction Mode:* Regulated using restricted pulse widths of 6.67 ms within the same period, establishing the structural 3.33 ms non-conducting gap between upper and lower devices.

3.2 Parametric Sweep Configuration

To evaluate the stability boundaries of the gating topologies under dynamic operating conditions, multi-variable parametric sweeps are performed in PSpice. The first sweep channel deviates the fundamental operating frequency across three discrete steps: 40 Hz, 50 Hz (nominal baseline), and 55 Hz. The second independent sweep channel scales the active gating pulse width from 6 ms to 12 ms against the 10 ms nominal timing. These sweeps are automated to systematically assess the tolerance of output voltage envelopes while holding other parameters constant.

3.1 Piecewise Linear (VPWL) Setup

An independent modulation channel is established by replacing the periodic pulse generators with open-loop Piecewise Linear (VPWL) voltage sources. This configuration uses precise time-voltage coordinate pairs in the

PSpice property matrix to define custom, non-uniform switching transitions. The VPWL setup is implemented to test the synchronization limits of the inverter bridge and to investigate how the open-loop system reacts to non-periodic gating signals.

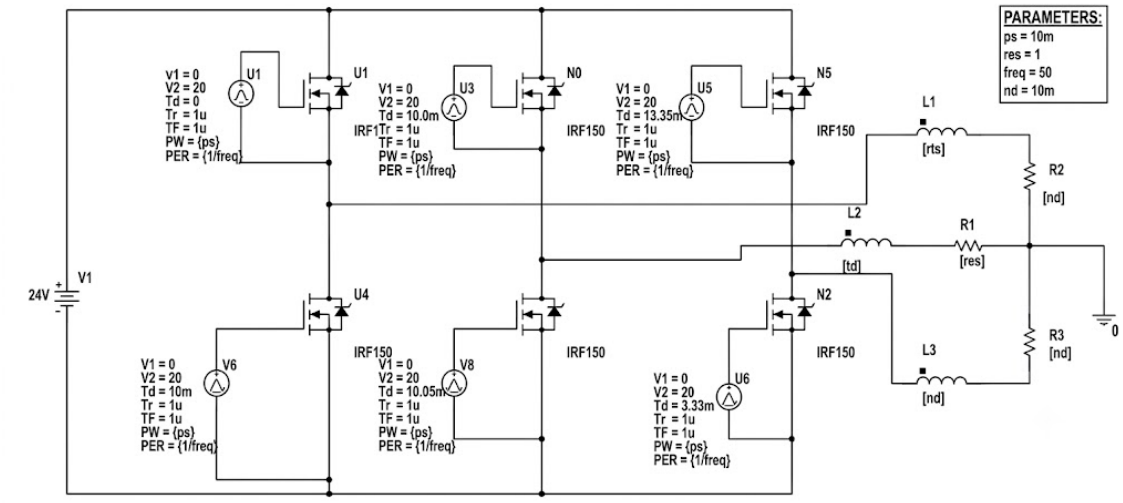

Fig. 4. Schematic diagram of the three-phase VSI connected to R-L load

4. RESULT AND ANALYSIS

4.1 Evaluation of Conduction Modes Under Variable Load Impedance

The time-domain simulation waveforms indicate geometric stability between the two conduction topologies as the load line reactance varied. In the 180° conduction mode, the line-to-line output voltage (Vab) consistently tracks a stable, balanced three-step quasi-square-wave profile as shown in Fig. 5. This geometric envelope is preserved across all testing quadrants from Case 1 through Case 4, proving that the continuous 180° firing pattern is highly immune to variations in load impedance. However, because complementary upper and lower switches on the same phase leg transition instantaneously without an implicit delay, this topology poses a severe risk of phase-leg shoot-through short circuits if gating pulses overlap, matching the safety vulnerabilities [6].

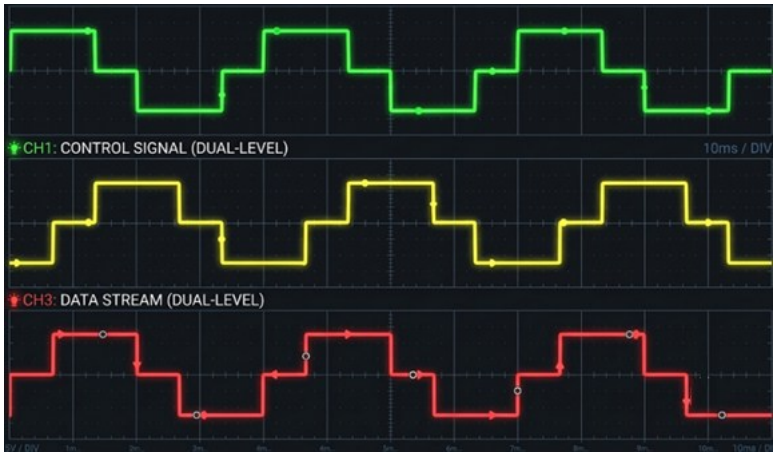

Fig. 5. Line-to-line output voltage (Vab) waveform under 180° conduction mode for Case 1.

The 120° conduction mode exhibits extreme sensitivity to load variations. In Case 1, the line voltage yields a clean staircase pattern with minor geometric distortion, providing a smoother transition that approaches a sinusoidal envelope as depicted in Fig. 6. When subjected to Case 2 (R = 10 Ω, L = 1 mH), severe switching instability occurs, where the line voltage exhibits high-amplitude peak voltage spikes at every switching edge as shown in Fig. 6. Under Case 3 (R = 1 Ω, L = 10 mH), the increased inductive reactance acts as a natural filter,

damping these transient spikes to yield an ideal staircase-step envelope. However, under Case 4 (R = 10 Ω, L = 10 mH), the active voltage steps become completely deformed and collapse into an asymmetric triangular waveform as observed in Fig. 7. This structural degradation occurs because the heavy inductive load stores significant reactive energy, forcing continuous current to flow through the antiparallel freewheeling diodes during the designated 60° non-conducting window. nder heavy inductive loads, the active voltage steps collapse into an asymmetric triangular waveform, confirming structural degradation [3].

Fig. 6: Three-phase line voltage waveforms in 120° conduction mode under (Case 1)

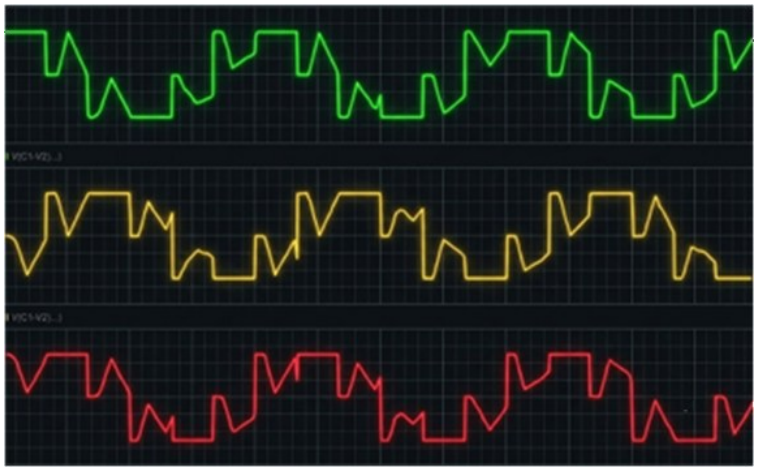

Fig. 7 Geometric collapse of line-to-line voltage (Vab) into a triangular profile under 120° conduction mode for Case 4.

4.2 Parametric Sweeps of Frequency and Pulse Width Channels

Deviating the operating frequency from the nominal 50 Hz baseline significantly limits power quality across variable inductive loads (L = 1 mH to L = 100 mH). Under the low-inductance profile (L = 1 mH), operating at the lower channels of 40 Hz and 45 Hz induces minor transient ringing along the switching edges as observed in Fig. 8. When the inductance is stepped up to 10 mH, an overall improvement is observed, with the waveform becoming exceptionally smooth at 50 Hz and 55 Hz. However, under a heavy load inductance of 100 mH, the output waveform at the 40 Hz channel exhibits severe transient ringing along the transition boundaries, indicating an unstable operating zone that the drive system must actively avoid.

Varying the gating pulse width shows that shorter durations (6 ms and 8 ms) reduce the effective root-mean-square (RMS) output voltage, producing clean but narrow voltage blocks that lower torque production. At the nominal 10 ms duration, the waveform yields a highly stable, symmetrical three-step quasi-square profile under baseline conditions. However, expanding the pulse width to 12 ms under low inductance forces the waveform to experience severe transient ringing at the switching boundaries, making it an unsatisfactory configuration. In contrast, under higher load conditions (L = 10 mH and L = 100 mH), the 120 ms expanded width successfully

widens the active steps while perfectly preserving a uniform, symmetrical transition with minimal distortion.

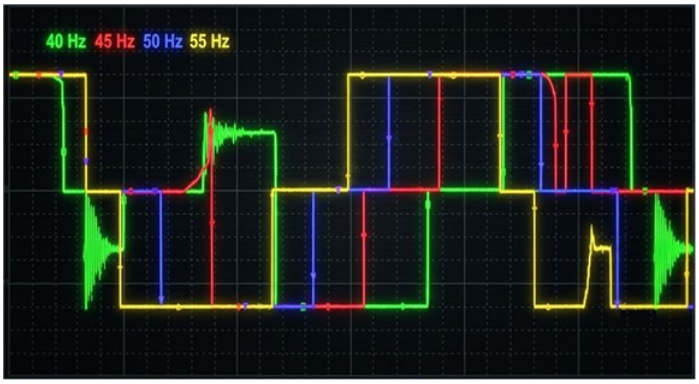

Fig. 8: Line voltage characteristics under frequency scaling (40 Hz - 55 Hz) with 100 mH

Varying the gating pulse width shows that shorter durations (6 ms and 8 ms) reduce the effective root-mean-square (RMS) output voltage, producing clean but narrow voltage blocks that lower torque production. At the nominal 10 ms duration, the waveform yields a highly stable, symmetrical three-step quasi-square profile under baseline conditions. However, expanding the pulse width to 12 ms under low inductance forces the waveform to experience severe transient ringing at the switching boundaries, making it an unsatisfactory configuration. In contrast, under higher load conditions (L = 10 mH and L = 100 mH), the 120 ms expanded width successfully widens the active steps while perfectly preserving a uniform, symmetrical transition with minimal distortion as observed in figures 9 and 10.

Fig. 9 Line voltage characteristics under pulse width (6 ms – 12 ms) with 1 mH

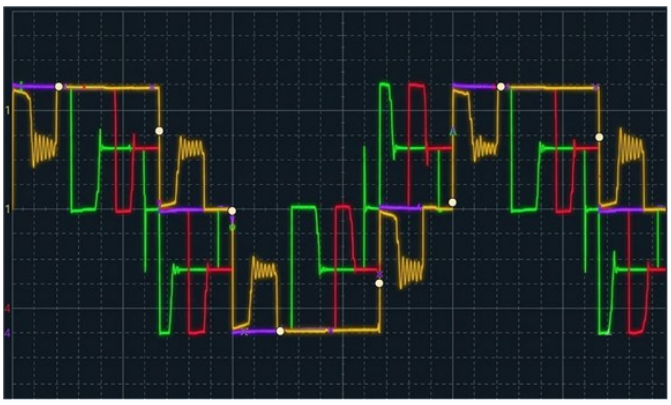

Fig. 10: Line voltage characteristics under pulse width (6 ms – 12 ms) with 100 mH

4.3 Evaluation of VPWL Modulation Stability

The implementation of coordinate-based VPWL inputs without a closed-loop feedback network proved highly ineffective for three-phase drive control. Due to the lack of strict time synchronization during non-uniform transitions, the independent gating pulses experienced severe phase overlap and timing collisions. This structural breakdown triggered continuous, high-frequency edge noise and heavy higher-order harmonic injection, confirming that open-loop VPWL controls are entirely unsuitable for secure vehicle traction operations, as observed in Fig. 12.

Fig. 12: Gate control signal overlaps and waveform switching collisions under VPWL coordination

5. CONCLUSION

This study has successfully mapped the strict operational boundaries, performance trade-offs, and geometric deformation limits of three-phase VSI gating strategies for EV applications using PSpice. The 180° mode provides superior line-voltage stability under dynamic loads but poses severe shoot-through risks. The 120° mode provides an inherent safety dead-time window that eliminates shoot-through paths, and VPWL coordination is verified as unviable due to gating overlaps. Future research will focus on integrating closed-loop Proportional-Integral-Derivative (PID) feedback networks to effectively minimize total harmonic distortion (THD) under high-power EV drive demands.

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