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Ferroelectric behavior and NCFETs - TCAD Simulation

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Abstract— With the miniaturization of transistors, the current leakage also increases due to the increasing tunnelling effect. Plus, Boltzmann's tyranny limits the subthreshold swing to be best and ideal at 60 mV/decade. Due to these, the power consumption in transistors keeps soaring up. Therefore, in this paper, the Negative Capacitance Effect Field Transistor (NCFET) is discussed as it possesses excellent potentials in reducing the power consumption in transistors. The negative capacitance induced in NCFET enables the internal voltage amplification and reduces the required voltage for the transistor to operate, and therefore, the power consumption is reduced. The literature reviews are done to gain knowledge on the structure and behavior of the NCFET. Next, the process and device simulation of NMOS are studied using Silvaco TCAD to get the idea of developing a circuit simulator model of NCFET. After that, we developed the circuit model of NCFET and MOSFET. Next, the ferroelectric parameters are varied to study how it will affect the ferroelectric material's polarization and capacitance. The ferroelectric thickness and source-drain doping concentration of the proposed NCFET model is also varied to study the NCFET behaviors in peak current, subthreshold slope, saturation current and saturation slope. Lastly, the performances of NCFET and MOSFET are compared. It is found that the NCFET has better performance as compared to the MOSFET as the NCFET can achieve a steeper subthreshold slope.

Keywords: *MOSFET, NCFET, Subthreshold slope, Ferroelectric, TCAD*

1. INTRODUCTION

The power consumption issue has merged to become a significant concern in CMOS technology. The Negative Capacitance Field Effect Transistor (NCFET) introduced in 2008 by S. Salahuddin is a promising candidate for solving the issue [1]. The negative capacitance exhibits by the ferroelectric in NCFET enables the voltage gate applied to be amplified, thus reducing the power consumption while maintaining the transistor's performance. The negative capacitance is utilized to overcome the Boltzmann mechanics that limit the subthreshold swing at 60 mV/decade. Many NCFET related works have been conducted to study the NCFET performance under different conditions [2-6].

Over the last few decades, shrinking the transistor is one of the implemented alternatives to achieve higher speed, improved power consumption and integration density [7]. However, after considering the conflicts mentioned above, it is worth mentioning that merely downsizing the transistors is no longer applicable. This is where the Negative Capacitance Field-Effect-Transistor (NCFET) is discovered to be one of the promising solutions to solve the issues.

In this paper, ferroelectric behavior and NCFETs behavior will be analyzed using TCAD simulation to observe the devices' performance.

2. BACKGROUND OF NEGATIVE CAPACITANCE

Electrostatic energy density in a dielectric material is given by

$$w = \int_0^D E(D)dD \qquad (1)$$

where E is the electric field and D is the electric displacement field. The relationship between E and D can be

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either linear or nonlinear. The total energy stored in a capacitor is given by

$$w = \int_0^Q V(Q)dQ \tag{2}$$

Where V is the applied voltage and Q is the charge stored in electrodes. The stored energy can be shown in Fig. 1a for a linear positive capacitance, C=dQ/dV, and energy stored in a capacitor is given by $w = CV^2/2$. However, for negative capacitance (NC) material, Q and V are not linear for all applied voltage, as shown in Fig. 1(b). Capacitor with negative differential capacitance dQ/dV < 0 due to dD/dE < 0.

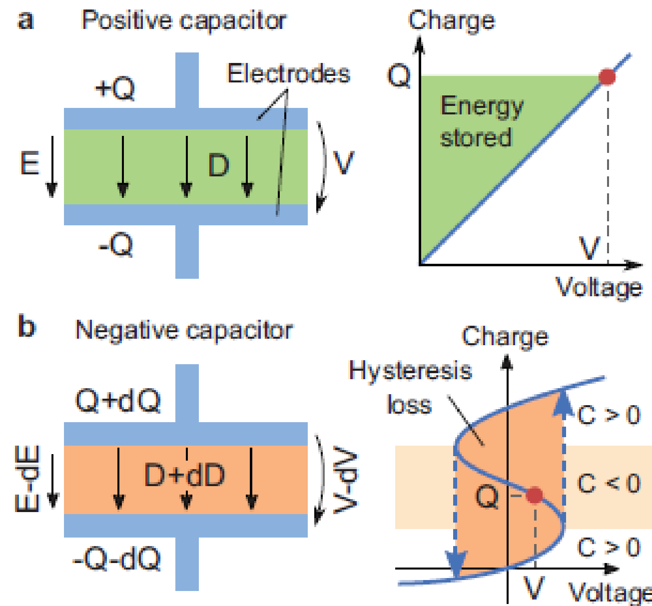

Fig. 1. (a) Positive and (b) Negative capacitances C-V characteristics [8].

2.1 *Ferroelectric negative capacitance to reduce subthreshold swing*

MOSFET with simple capacitance divider as shown in Fig. 2. V_G is the applied gate voltage, C_{ox} and C_S are the oxide and semiconductor capacitance, respectively.

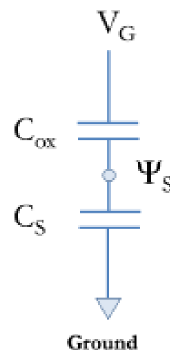

Fig. 2. A simplified view of a MOSFET as a capacitive divider.

The surface potential ψ_s is related to gate voltage as

$$\psi_s = \frac{C_{ox}}{C_{ox} + C_s} V_G \tag{3}$$

The surface potential and gate voltage is denoted by "body factor", m and is given by

$$m^{-1} = \frac{\delta\psi_s}{\delta V_G} = \left(1 + \frac{C_s}{C_{ox}}\right)^{-1} \quad (3)$$

The subthreshold slope (SS) is defined as $\delta V_G/\delta log_{10}(I_D)$ which can be written as

$$SS^{-1} = \frac{\delta log_{10}(I_D)}{\delta V_G}\frac{\delta log_{10}(I_D)}{\delta\psi_s}\frac{\delta\psi_s}{\delta V_G} = \frac{1}{log_{10}}\frac{q}{k_B T}\frac{1}{1+\frac{C_s}{C_{ox}}} \quad (4)$$

It can be seen that the functional form of m and SS, negative oxide capacitance amplifies the surface potential relative to the gate voltage, thus reducing the body factor below m and reducing SS slope below 60mV/decade. Ferroelectric materials are used to realized negative capacitance. A ferroelectric is defined as a material that exhibits a spontaneous polarization that can be reversed with an applied electric field. The polarization characteristics of ferroelectric materials are shown in Fig. 3.

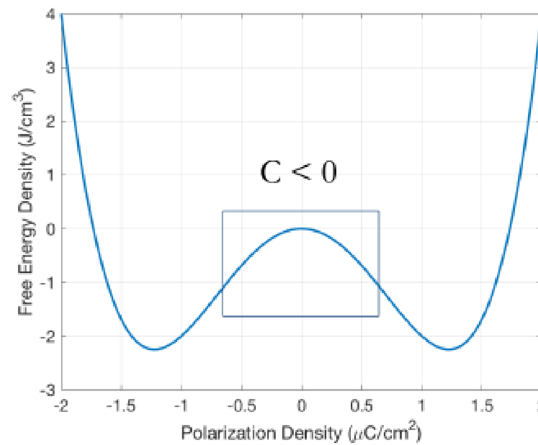

Fig. 3. Polarization density of ferroelectric material with a distinct negative capacitance zone.

Recently, researchers capture an image of negative capacitance in action [9]. They have shown fundamental, atomistic insight into the physics of negative capacitance. They have shown NC behavior in $SrTiO_3/PbTiO_3$ heterostructure system.

2.2 NCMOSFET

Fig. 4 shows the realization of NCMOSFET proposed by Kobayashi et al. and shows the performance of the device. The structure of a NCFET is the same as a MOSFET, except that the gate insulator is replaced by a ferroelectric material, as shown in Fig. 4.

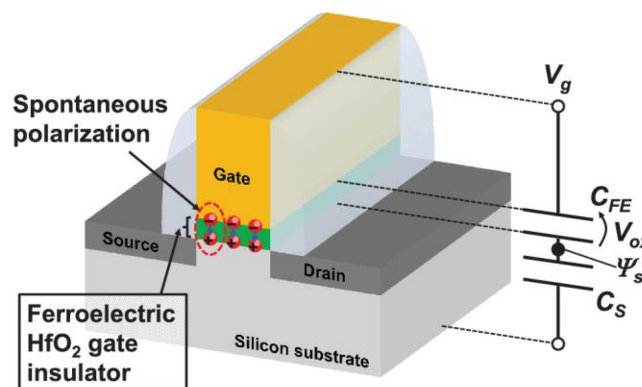

Fig. 4. A schematic of a NCFET with a ferroelectric gate insulator. A ferroelectric MOS capacitor is modeled by series connection of ferroelectric and channel capacitance [10]

Alam *et al.* recently critically review the progress on negative capacitance [11]. He has summarized the findings in Fig. 5.

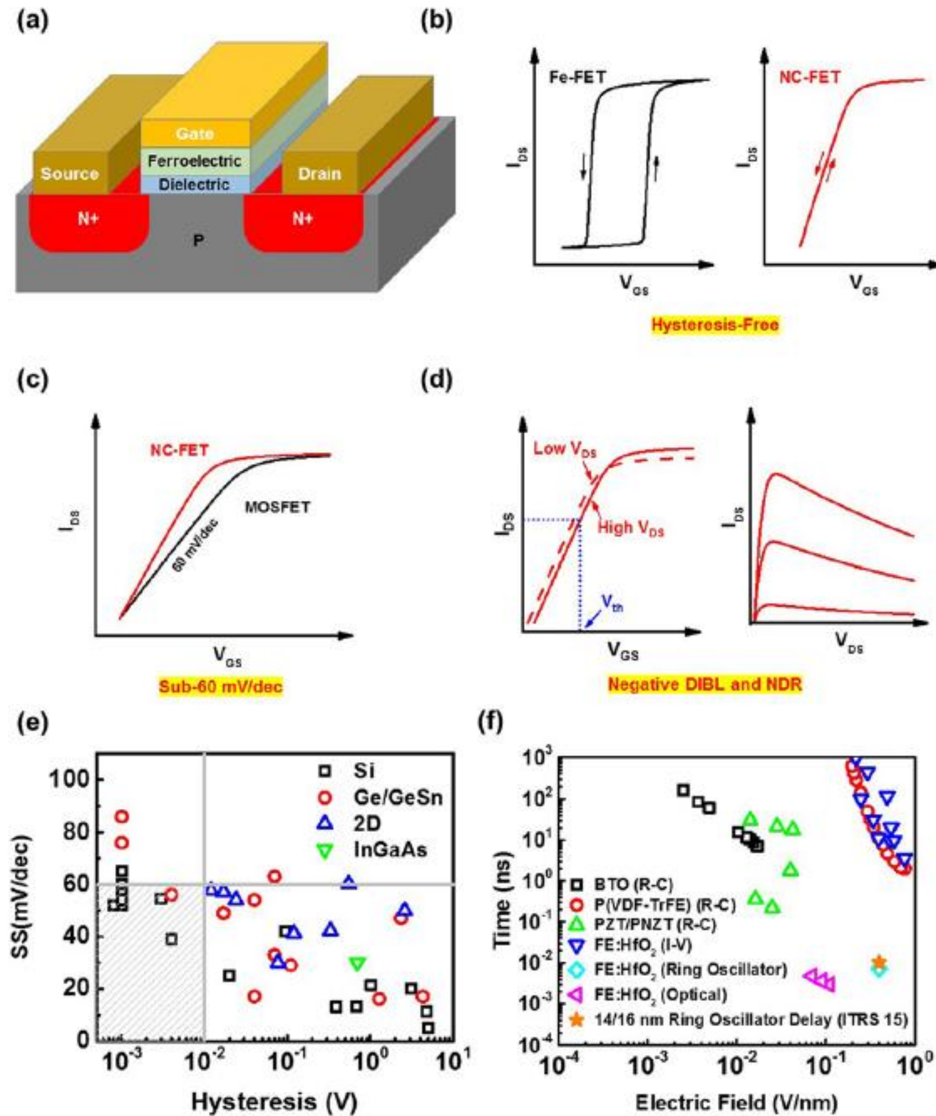

Fig. 5. (a) Schematic image of a NC-FET with ferroelectric and conventional dielectric as the gate stack. (b) The fundamental difference in transfer characteristics of a Fe-FET versus a NC-FET which has an anti-clockwise hysteresis or zero hysteresis, respectively. (c) Expected steep-slope less than 60 mV/dec at room temperature for a NC-FET. (d) Expected negative DIBL and negative drain resistance for a NC-FET. (e) Summary of the reported representative data in the literature in terms of SS versus hysteresis in transfer characteristics (SiGe/GeSn, 2D, InGaAs). SS is plotted as the larger SS in forward and reverse gate sweeps and only when both are available. Data without explicitly reported hysteresis are plotted with 1mV hysteresis. (f) Summary of reported switch times of representative ferroelectric films versus the electric field by different characterization methods in the literature (BTO (R-C), PZT/PNZT (R-C), P(VDF-TrFE) (R-C), FE:HfO2 (I-V), FE:HfO2 (ring oscillator), FE:HfO (optical)) [11].

The author also mentioned different types of experiments to support negative capacitances.

3. RESULTS AND DISCUSSION

3.1 The Ferroelectric Behavior

To characterize the proposed NCFET model, it is important to first acknowledge the behavior of the ferroelectric based on its parameters' variation. There are four ferroelectric parameters which are the electric field (E_c), permittivity (*esf*), spontaneous polarization (P_S) and remnant polarization (P_r). Figures 6-9 show the capacitance and polarization vs gate bias with varied *esf*, P_S, P_r and E_c, respectively.

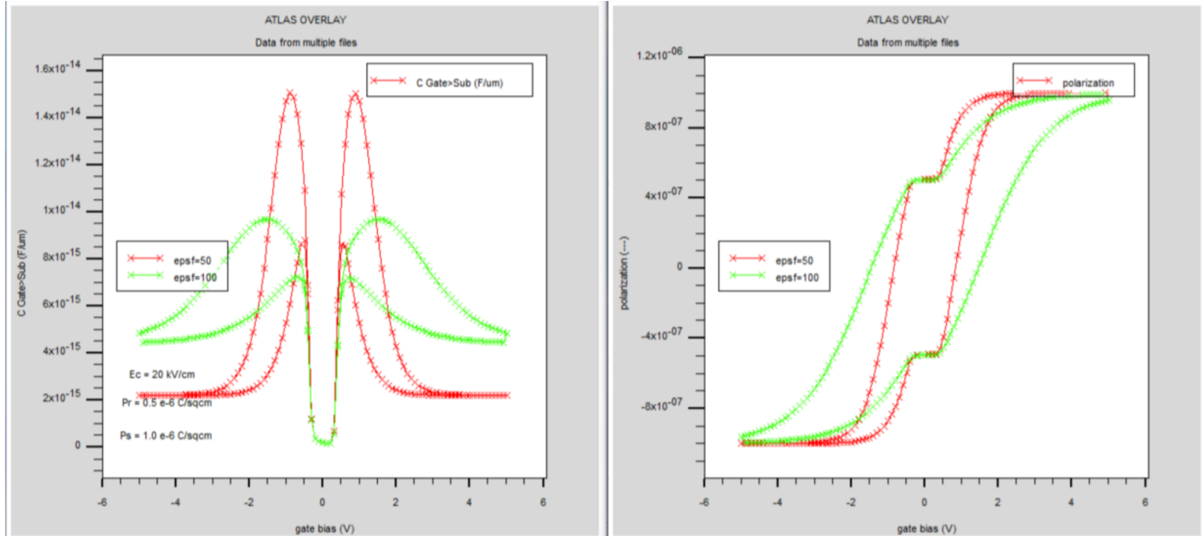

Fig. 6. The capacitance and polarization vs gate bias for *esf* = 50 and *esf* = 100

Figure 6 shows the capacitance and the ferroelectric polarization curve when the *esf* parameter is varied at 50 and 100, while other parameters are made constant (P_r = 0.5μC/cm^2, P_S = 1μC/cm^2, E_c = 20 kV/cm). The figure shows that the 100-*esf* ferroelectric exhibits higher capacitance and thinner hysteresis loop as compared to that of 50-*esf* ferroelectric.

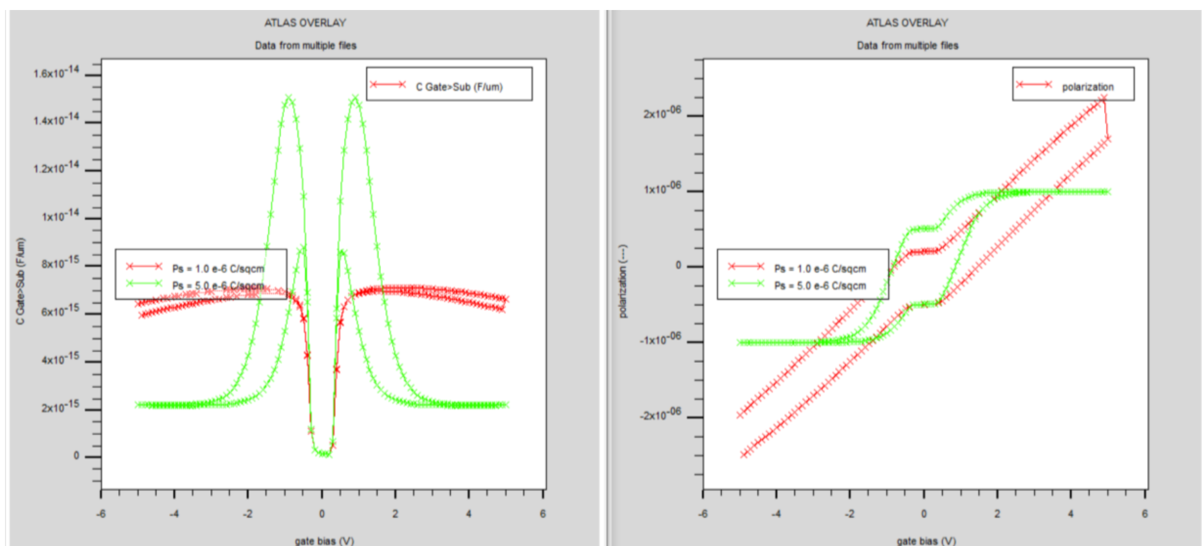

Fig. 7. The capacitance and polarization vs gate bias for P_S = 1μC/cm^2 and P_S = 5μC/cm^2

Figure 7vshows the capacitance and the polarization curve of the ferroelectric when the P_S parameter is varied

at 1µC/cm^2 and 5µC/cm^2, while other parameters are made constant (esf = 50, P_r= 1µC/cm^2, E_c = 20 kV/cm). From the figure, it can be concluded that as the P_S parameter increases, the ferroelectric capacitance also increases, and the hysteresis loop becomes smaller.

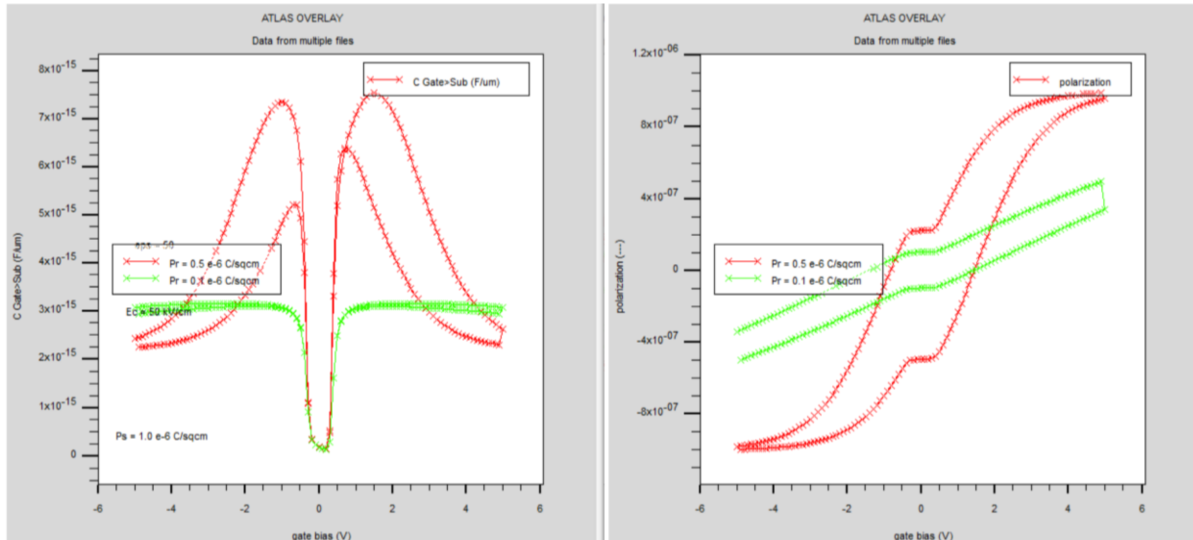

Fig. 8. The capacitance and polarization vs gate bias for P_r =0.5µC/cm^2 and P_r =0.1µC/cm^2

Figure 8 shows the capacitance and the polarization curve of the ferroelectric when the P_r parameter is varied at 0.5µC/cm^2 and 0.1µC/cm^2, while other parameters are made constant (esf = 50, P_S = 1µC/cm^2, E_c = 50 kV/cm). From the figure, it is observed that each different P_r yields a very different shape of the hysteresis loop and the 0.5µC/cm^2-P_r ferroelectric exhibits much higher capacitance as compared to the 0.1µC/cm^2-P_r ferroelectric.

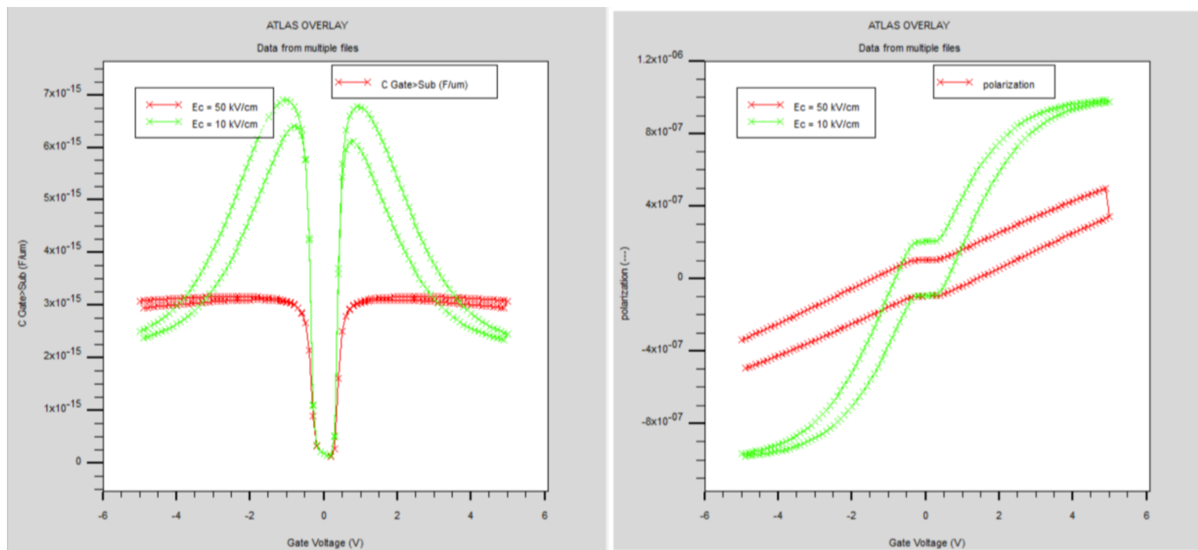

Fig. 9. The capacitance and polarization vs gate bias for E_c = 50 kV/cm and E_c=10 kV/cm

Figure 9 shows the capacitance and the polarization curve of the ferroelectric when the E_c parameter is varied at 50 kV/cm and 10 kV/cm, while other parameters are made constant (esf = 50, P_S = 1µC/cm^2, P_r = 0.1µC/cm^2). From the figure, it is found that the 50 kV/cm-E_c ferroelectric produces a thin hysteresis loop and high capacitance.

In short, the ferroelectric parameters are affecting the capacitance and polarization behavior of the ferroelectric material. Therefore, it is better to choose suitable ferroelectric parameters to achieve a better capacitance matching between the ferroelectric and dielectric capacitor.

3.2 The NCFET Structure for TCAD Simulation

Figure 10 shows the structure of the proposed NCFET compared to MOSFET. The MOSFET consists of two layers, which are the substrate and one dielectric layer, as shown in Figure 4.6a, while the NCFET consists of 4 layers as shown in Figure 4.6b. Table 4.1 lists the NCFET parameters.

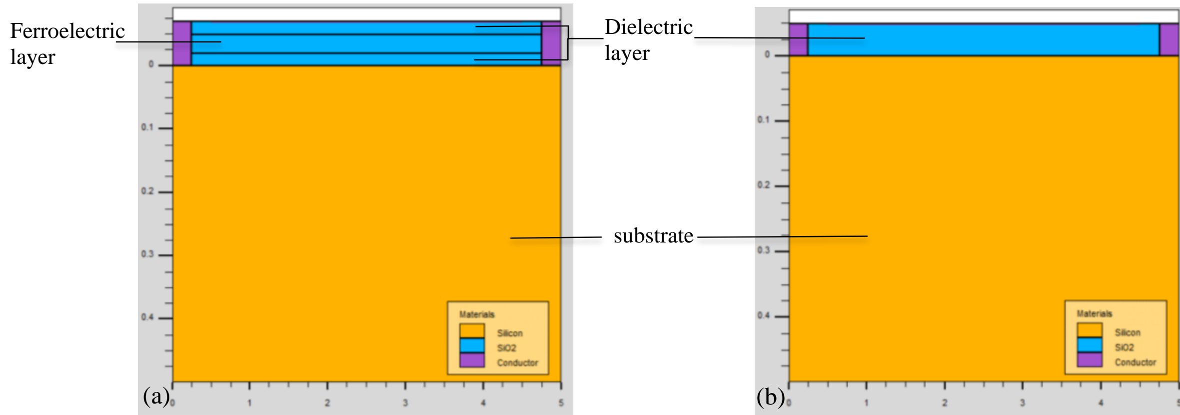

Fig. 10. The proposed structure of (a) NCFET and (b) MOSFET.

Table 1. The proposed NCFET and MOSFET parameters.

Parameter (unit)	NCFET
p-well doping concentration (cm^{-3})	$1x10^{19}$
Source-drain doping concentration (cm^{-3})	$1x10^{19}$
Substrate doping concentration (cm^{-3})	$3x10^{16}$
Dimension (μm x μm)	5x5
Gate length, L_g (nm)	4.5
Dielectric material	SiO_2
Ferroelectric material	E_C=1.2 MV/cm Pr=12.5e μC/cm^2 P_S=13.24 μC/cm^2 esf=35.5
Dielectric material	SiO_2
Dielectric thickness (nm)	0.02

As can be seen from Table 1, the chosen ferroelectric parameters are E_c=1.2MV/cm, P_r=12.5e μC/cm^2, P_S=13.24 μC/cm^2 and esf=35.5 for our NCFET model. On top of that, both devices' gate length is set to be 4.5nm to avoid any short-channel effect [12].

3.1.1 The Effect of Ferroelectric Thickness on the NCFET Performance

For this set of experiments, the ferroelectric layer's thickness is varied while all other parameters are made fixed, including the source-drain doping concentration of $1x10^{19}cm^{-3}$. The NCFET structures with the different ferroelectric thickness of 5nm, 10nm, 20nm and 30nm, and their I-V characteristics are depicted in Figure 11,12,13 and 14, respectively.

For all the I_D vs V_{DS} plot depicted in this project, there are three different applied gate voltages which are 1.1V, 2.2V and 3.3V and their curves are shown by the red, green, and blue curve, respectively. The drain voltage is then supplied until 5.5V with the step of 0.3V. Next, for the I_D vs V_g plot, the drain voltage is biased with 0.025V and the gate voltage is ramped from 0 to 1V with the step of 0.1V.

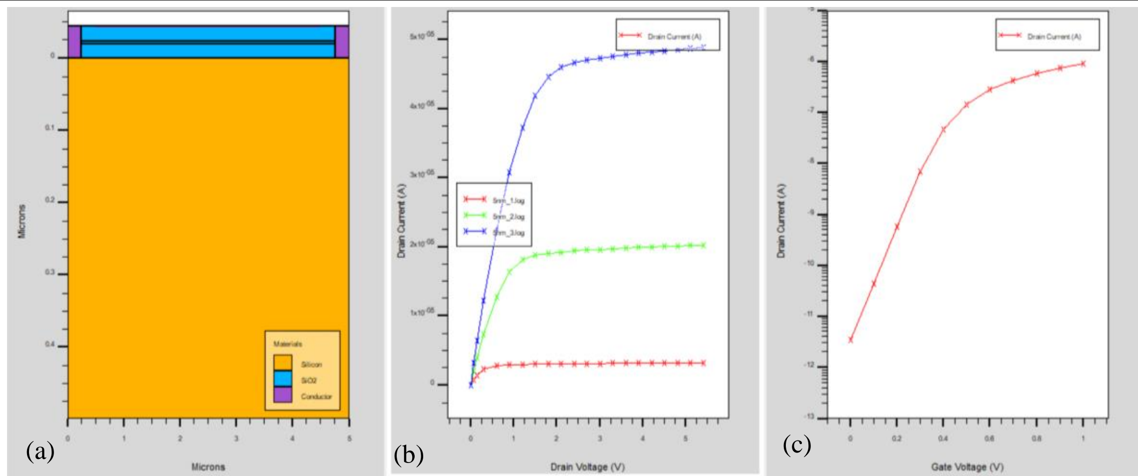

Fig. 11. Variation of drain current, I_D versus (b) Drain voltage, V_{DS} (c) Gate voltage, V_g of **5** nm thick ferro NCFET.

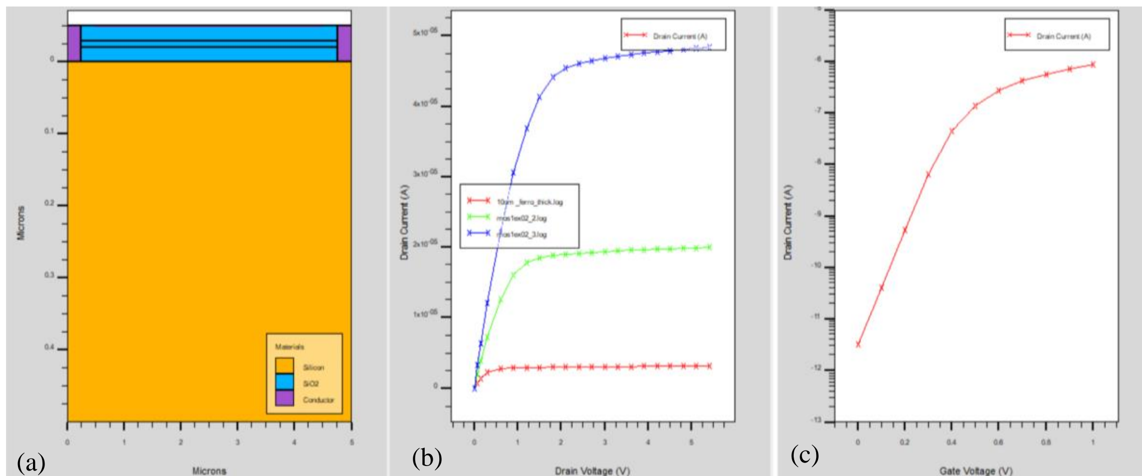

Fig. 12. Variation of drain current, I_D versus (b) Drain voltage, V_{DS} (c) Gate voltage, V_g of 10 nm-thick ferro NCFET.

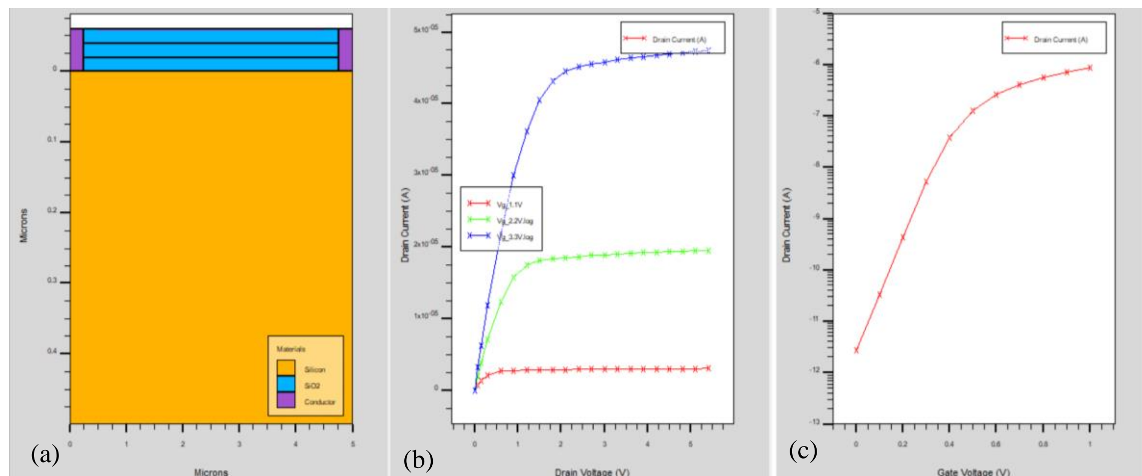

Fig. 13. Variation of drain current, I_D versus (b) Drain voltage, V_{DS} (c) Gate voltage, V_g of 20 nm-thick ferro NCFET.

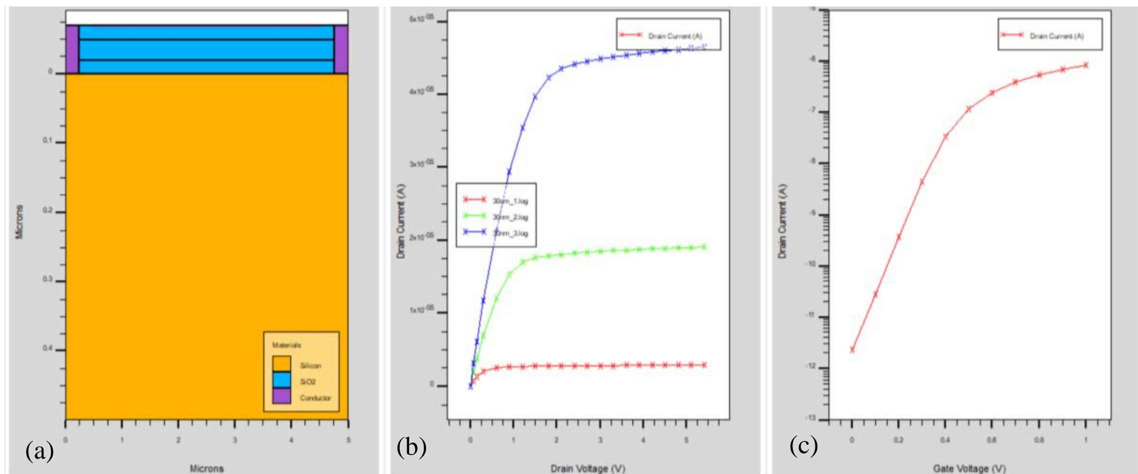

Fig. 14. Variation of drain current, I_D versus (b) Drain voltage, V_{DS} (c) Gate voltage, V_g of 30nm-thick Ferro NCFET.

From the results shown in Figure 11 until Figure 14, it shows that all the NCFET with different ferroelectric thickness are following the MOSFET I-V characteristic. Next, the behaviors of the NCFET in terms of peak current, saturation slope, saturation current and subthreshold slope are summarized in Table 2.

Table 2: The NCFET electrical behaviors with different ferroelectric thickness.

Ferroelectric thickness (nm)	Peak Current (mA)	Saturation Slope (μA/V)	Subthreshold slope with bias drain voltage = 0.025 V (mV/dec)	Voltage Gate (V)	Saturation Current (mA)
5	0.04889	0.4615	89.102	1.1	0.003212
				2.2	0.020251
				3.3	0.048877
10	0.04837	0.4623	89.3754	1.1	0.003147
				2.2	0.02
				3.3	0.048364
20	0.04742	0.467	89.9125	1.1	0.003031
				2.2	0.019542
				3.3	0.047424
30	0.0465	0.47366	90.4744	1.1	0.002917
				2.2	0.019094
				3.3	0.0465

Figure 15 depicts the relationship between the peak current and the saturation slope with the ferroelectric thickness. From the figure, it is found that as the ferroelectric thickness increases, the peak current decreases, whereas the saturation slope is increasing with the ferroelectric thickness, although there is not much difference between the slope values.

Figure 16 shows the relationship between the subthreshold slope and ferroelectric thickness. The plot shows that the subthreshold slope is directly proportional to the ferroelectric thickness. In terms of subthreshold slope, the best performance is achieved by the 5nm-thick ferroelectric NCFET as it achieves the steepest slope of 89.10mV/dec. As in equation (5), when the ferroelectric thickness (T_{FE}) increases, the ferroelectric capacitance (C_{FE}) decreases, which makes it closely match the C_{MOS}. The enhanced matching between the C_{MOS} and the $C_{FE}(|C_{FE}|-C_{MOS}>0)$ then increases the voltage amplification factor, A_G. The voltage amplification factor and the subthreshold slope have a negative correlation, which implies that the higher the ferroelectric thickness, the steeper the subthreshold slope.

$$C_{FE} = \frac{dQ}{dV_{FE}} = \frac{1}{2\alpha T_{FE}} = \frac{2}{3\sqrt{3}} \frac{P_r}{E_C T_{FE}} \tag{5}$$

$$A_G = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{6}$$

$$SS = 60\, x \left(1 + \frac{C_{dm}}{C_{ox}}\right) x \frac{1}{A_G} \tag{7}$$

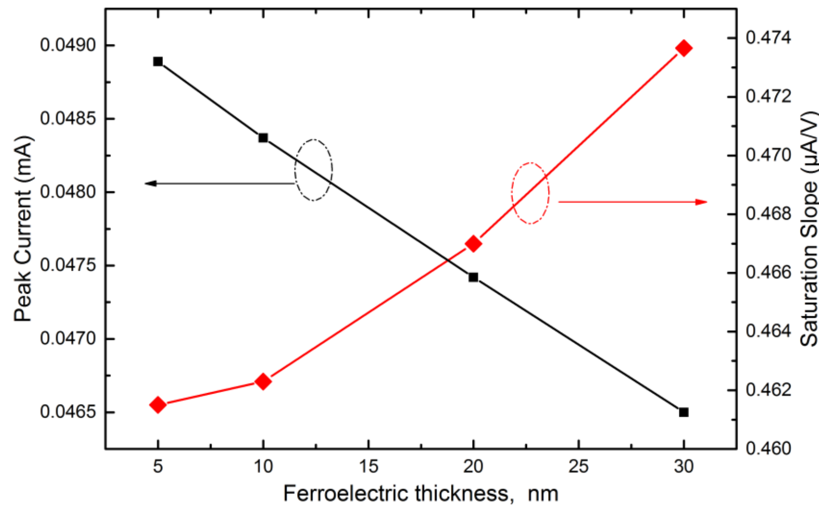

Fig. 15. Peak current and the saturation slope vurses ferroelectric thickness

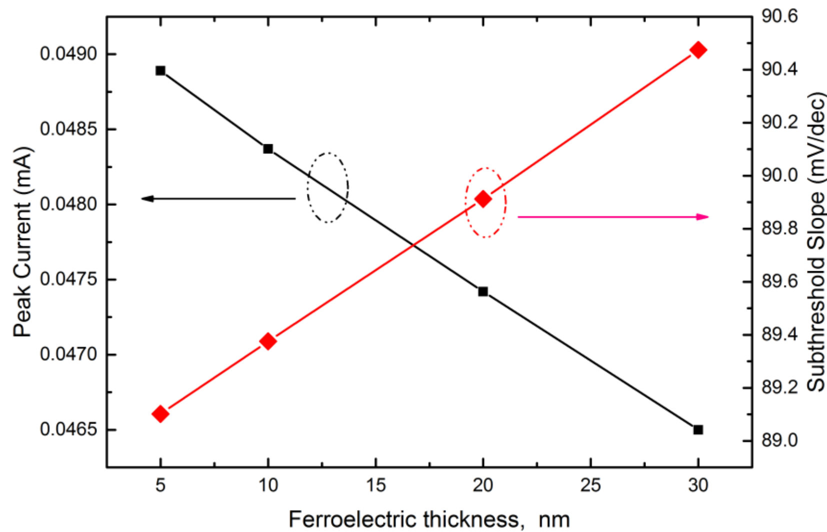

Fig. 16. Subthreshold slope versus ferroelectric thickness.

Figure 17 shows the relationship between the peak current and the subthreshold slope with the source-drain doping concentration. The figure shows that the peak current is directly proportional and the subthreshold slope is inversely proportional to the source-drain doping concentration. The higher the doping concentration, the greater the depletion capacitance (C_{dm}), the greater the increases in C_{dm}/ C_{FE} as compared to the C_{dm}/C_{ox}, and thus, the steeper the subthreshold slope. However, noticed that the subthreshold slope, SS is not less than 60 mV/dec as it supposed to be as according to equation (8), the absence of proper fabrication processes and other ignored variables.

$$SS = 60\,x\,(1 + \frac{C_{dm}}{C_{ox}} - \frac{C_{dm}}{|C_{FE}|}) \quad (8)$$

Where C_{dm} = Depletion capacitance, C_{ox} = Gate oxide capacitance

Therefore, it is found that by increasing the source-drain doping concentration in the proposed NCFET model, the subthreshold slope can be made steeper.

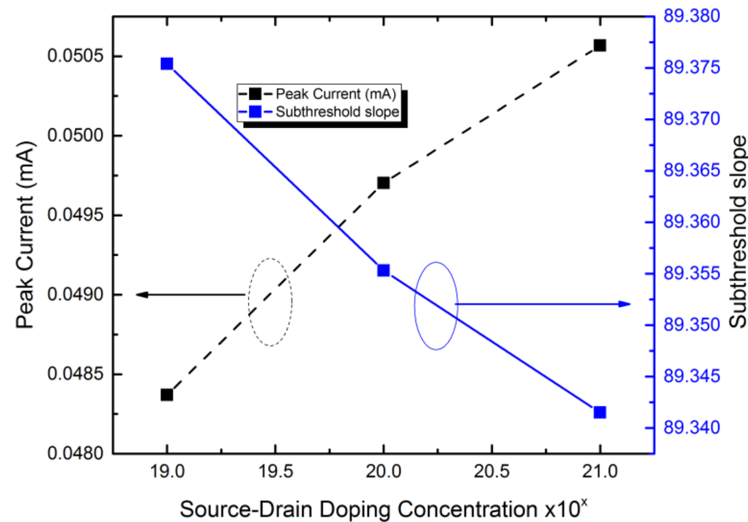

Fig. 17. Subthreshold slope vurses source-drain doping concentration.

4. CONCLUSION

The effects of ferroelectric parameters (electric field (E_c), permittivity (*esf*), spontaneous polarization (P_S) and remnant polarization (P_r)) are studied on its capacitance and polarization behaviors. Next, the structure and parameters of the proposed NCFET is presented. The effects of the ferroelectric thickness and source-drain doping concentration on the proposed NCFET and MOSFET behavior are demonstrated. It is proved that the NCFET has better performance as it achieved a steeper subthreshold slope.

The results show that as the ferroelectric thickness increases, the peak current and the saturation current are decreasing while the saturation slope and subthreshold slope are increasing. Next, in terms of the source-drain doping concentration, the peak current, saturation current, and saturation slope are increasing with the source-drain doping concentration, while the subthreshold slope is inversely proportional to the doping concentration.

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